REMARKS

Claims 12 and 14-17 are pending in this application. All claims have been rejected under 35 U.S.C. §112, second paragraph as being indefinite and under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,448,586 (Nemati) in view of U.S. Patent No. 5,357,125 (Kumagi).

In making the indefiniteness rejection, the Examiner states that "the gate is a separate, stand alone part of the Thin-Film Transistor (TFT) and it is the TFT that includes the source/drain and the body".

It should first be noted that the inventive claims are directed to an array of planar T-RAM cells (see numeral 300 in FIG. 14) where each T-RAM cell (see numeral 200 in FIGs. 12-14) includes a buried vertical thyristor (see numeral 210 in FIG. 13) and a horizontally stacked pseudo-TFT transfer gate (see numeral 220 in FIG. 13). The transfer gate is a **pseudo-TFT**, and not a TFT as the Examiner maintains. The Merriam-Webster dictionary describes the word pseudo as "being apparently rather than actually as stated". It is also noted that the array of planar T-RAM cells (see numeral 300 in FIG. 14) of the present invention is a singe structure on a single crystal TFT.

Furthermore, the inventive specification and claims refer to a horizontally stacked pseudo-TFT transfer gate. In this use, the word "gate" should not be confused with a gate of a transistor. The horizontally stacked pseudo-TFT transfer gate (220) of the present invention refers to **a transistor** that is positioned above and covers the entire top surface of a PNP thyristor (212). The transistor 220 comprises a source/drain (132a, 132b), a body (area between 132a, 132b, FIG. 13), and a gate, which is the WLL1.

To clarify the recitation of the invention, Claim 12 has been amended to now state "a horizontally stacked pseudo-TFT transfer gate" where only the words transfer gate was previously used. Additionally, please refer to Fig. 13 of the present invention to see all referenced components. It is noted that the designation "a horizontally stacked pseudo-TFT transfer gate" is given to the transistor referenced by numeral 220 in Figs. 11-14. Moreover, please note the box identified by the letters "TGR" in Figs. 12 and 14. TGR designates the

transfer gate region of the horizontally stacked pseudo-TFT transfer gate 220.

As with regard to Nemati, the Examiner points to FIG. 8 of Nemati as teaching the elements of Claim 12. Specifically, FIG. 8 of Nemati shows a plurality of PNPN-type NDR devices, with respective control ports being provided by interconnected charge plates (or gates) 48 primarily adjacent to the upper N region of each PNPN-type NDR device.

In view of the discussion above regarding the nature of the horizontally stacked pseudo-TFT transfer gate of the present invention, such comparison is incorrect. A stacked pseudo-TFT transfer gate is not shown in Nemati; gate 48 is a control gate possibly equivalent to WLL1 or WLL2 of the present invention.

Kumagi does not add to the discussion. It can therefore be concluded that neither Nemati, Kumagi, nor the combination thereof teach or describe the limitations recited in independent Claim 12.

Applicants submit that independent Claim 12 is believed to be in condition for allowance, Since Claims 14-17 are dependent from Claim 12, they are as well believed to be in condition for allowance for the same reasons. Allowance is respectfully requested.

Should the Examiner believe that a telephone conference or personal interview would facilitate resolution of any remaining matters, the Examiner may contact Applicants' attorney at the number given below.

Respectfully submitted,

Paul J. Farrell
Reg. No. 33,494
Attorney for Applicants

DILWORTH & BARRESE, LLP
333 Earle Ovington Blvd.
Uniondale, New York 11553
Tel: (516) 228-8484